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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,949	10/08/2003	William M. Hurley	2003.10.008.WS0	6032

7590 01/31/2007

Docket Clerk
P.O. Box Drawer 800889
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EXAMINER	
RUTZ, JARED IAN	
ART UNIT	**PAPER NUMBER**
2187	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	10/680,949	HURLEY, WILLIAM M.
	Examiner	Art Unit
	Jared I. Rutz	2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2006*.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-7,9-13 and 15-19* is/are rejected.
7)☒ Claim(s) *8, 14, and 20* is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a)☐ All b)☐ Some * c)☐ None of:
1.☐ Certified copies of the priority documents have been received.
2.☐ Certified copies of the priority documents have been received in Application No. _____.
3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 as amended on 1/30/2006 are pending in the instant application. The arguments contained in the Appeal Brief filed 9/21/2006 have been carefully and fully considered, and are found persuasive. The grounds of rejection presented in the Office action of 4/13/2006 and the **finality** of said Office action have been withdrawn. This Office action contains new grounds of rejection, not necessitated by Amendment of the claims. Accordingly, this Office action is non-final.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-6, 9-13, and 15-18** are rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al. (US 6,327,625).

4. **Claim 1** is taught by Wang as:

a. *For use in a digital device, a first-in, first-out memory apparatus comprising: a memory operable to store a data packet.* Column 4 lines 10-14 show that a packet is received by packet filter 14 and stored in FIFO 13.

b. *Circuitry operable to store a length of the data packet and the data packet in the memory.* Column 4 lines 14-19 shows that a frame start header 16 is stored in the FIFO. Column 7 lines 8-10 shows that the frame start header can store the packet length.

c. *And circuitry operable to flush the length and the data packet from the memory when the data packet is invalid.* Column 6 lines 40-48 show that when a packet is discarded because of runt packet detection or other processing causing uninteresting packets to be discarded, the write pointer is reset to the value of the beginning of packet pointer for the discarded packet, thereby flushing the invalid packet.

5. **Claim 2** is taught by Wang as:

d. *The apparatus as set forth in Claim 1, wherein: the length and data packet comprise a plurality of words.* Column 3 lines 17-37 show that the invention is directed to a computer networking device for receiving and transmitting data packets. As is known to one of ordinary skill in the art, data packets comprise a plurality of words.

e. *And the circuitry for storing the length and data packet in the memory comprises a first pointer operable to identify a location in the memory.* Column 4 lines 53-55 shows that write pointer WrPtr 56 is included to indicate where data written to the packet belongs.

f. *Wherein the first pointer is advanced for each word written to the memory.* Column 6 lines 34-41 shows that write pointer is incremented each time data is written to the packet.

6. **Claim 3** is taught by Wang as:

g. *The apparatus as set forth in Claim 2, wherein the circuitry for storing the length and data packet further comprises: a length unit operable to provide the length of the data packet.* Column 6 lines 30-34 shows that control block 22 writes a null frame start header when an incoming packet is detected.

h. *And a multiplexer operable to selectively provide each of the length and the data packet to the memory.* Column 4 lines 35-38 shows that multiplexer 29 is used to supply address and data signals from the currently active process to the FIFO.

7. **Claim 4** is taught by Wang as:

i. *The apparatus as set forth in Claim 2, wherein the circuitry for flushing the length and data packet from the memory comprises an additional pointer operable to identify the first location in the memory where one of the words is stored.* Column 4 lines 39-45 shows that beginning of packet pointer BopPtr 52 points to the beginning of the top packet frame start header 50 as shown in figure 2.

j. *The location identified by the additional pointer being used as the first pointer when the data packet is flushed.* Column 6 lines 45-48 shows that if a packet is discarded, the write pointer is reset to the value of the beginning of packet pointer for the discarded packet.

8. **Claim 5** is taught by Wang as:

k. *The apparatus as set forth in Claim 2, further comprising circuitry for retrieving the data packet from the memory.* Column 4 lines 39-47 shows that read pointer RdPtr 54 points to a location in the buffer for a current read process.

9. **Claim 6** is taught by Wang as:

l. *The apparatus as set forth in Claim 5, wherein the circuitry for retrieving the data packet comprises a second pointer operable to identify a location in the memory where a word is to be retrieved.* Column 4 lines 39-47 shows that read pointer RdPtr 54 points to a location in the buffer for a current read process.

10. **Claim 9** is taught by Wang as:

m. *A digital device comprising: at least one interface operable to receive and communicate data packets.* Column 4 lines 10-13 show that incoming data on port 11 is supplied to packet filter 14.

n. *And a first-in, first-out memory comprising: a memory operable to store a data packet.* Column 4 lines 10-14 show that a packet is received by packet filter 14 and stored in FIFO 13.

o. *Circuitry operable to store a length of the data packet and the data packet in the memory.* Column 4 lines 14-19 shows that a frame start header 16 is stored in the FIFO. Column 7 lines 8-10 shows that the frame start header can store the packet length.

p. *And circuitry operable to flush the length and the data packet from the memory when the data packet is invalid.* Column 6 lines 40-48 show that when a packet is discarded because of runt packet detection or other processing causing uninteresting packets to be discarded, the write pointer is reset to the value of the beginning of packet pointer for the discarded packet, thereby flushing the invalid packet.

11. **Claim 10** is taught by Wang as:

q. *The digital device as set forth in Claim 9, wherein: the length and data packet comprise a plurality of words.* Column 3 lines 17-37 show that the invention is directed to a computer networking device for receiving and transmitting data packets. As is known to one of ordinary skill in the art, data packets comprise a plurality of words.

r. *And the circuitry for storing the length and data packet in the memory comprises a first pointer operable to identify a location in the memory.* Column 4 lines 53-55 shows that write pointer WrPtr 56 is included to indicate where data written to the packet belongs.

s. *Wherein the first pointer is advanced for each word written to the memory.* Column 6 lines 34-41 shows that write pointer is incremented each time data is written to the packet.

12. **Claim 11** is taught by Wang as:

t. *The digital device as set forth in Claim 10, wherein the circuitry for storing the length and data packet further comprises: a length unit operable to provide the length of the data packet.* Column 6 lines 30-34 shows that control block 22 writes a null frame start header when an incoming packet is detected.

u. *And a multiplexer operable to selectively provide each of the length and the data packet to the memory.* Column 4 lines 35-38 shows that multiplexer 29 is used to supply address and data signals from the currently active process to the FIFO.

13. **Claim 12** is taught by Wang as:

v. *The digital device as set forth in Claim 10, wherein the circuitry for flushing the length and data packet from the memory comprises an additional pointer operable to identify the first location in the memory where one of the words is stored.* Column 4 lines 39-45 shows that beginning of packet pointer BopPtr 52 points to the beginning of the top packet frame start header 50 as shown in figure 2.

w. *The location identified by the additional pointer being used as the first pointer when the data packet is flushed.* Column 6 lines 45-48 shows that if a packet is discarded, the write pointer is reset to the value of the beginning of packet pointer for the discarded packet.

14. **Claim 13** is taught by Wang as:

x. *The digital device as set forth in Claim 10, further comprising circuitry for retrieving the data packet from the memory, the circuitry for retrieving the data packet comprising a second pointer operable to identify a location in the memory where a word is to be retrieved.* Column 4 lines 39-47 shows that read pointer RdPtr 54 points to a location in the buffer for a current read process.

15. **Claim 15** is taught by Wang as:

y. *For use in a digital device, a method for storing data in a first-in, first-out memory, comprising: receiving a data packet.* Column 6 lines 30-32.

z. *Storing a length of the data packet and the data packet in the first-in, first-out memory.* Column 6 lines 33-40.

aa. *And flushing the length and the data packet from the memory when the data packet is invalid.* Column 7 lines 2-6.

16. **Claim 16** is taught by Wang as:

bb. *The method as set forth in Claim 15, wherein: the length and data packet comprise a plurality of words.* Column 3 lines 17-37 show that the invention is directed to a computer networking device for receiving and transmitting data packets. As is known to one of ordinary skill in the art, data packets comprise a plurality of words.

cc. *And storing the length and data packet in the memory comprises using a first pointer operable to identify a location in the memory.* Column 4 lines 53-55 shows that write pointer WrPtr 56 is included to indicate where data written to the packet belongs.

dd. *Wherein the first pointer is advanced for each word written to the memory.* Column 6 lines 34-41 shows that write pointer is incremented each time data is written to the packet.

17. **Claim 17** is taught by Wang as:

ee. *The method as set forth in Claim 16, wherein flushing the length and data packet from the memory comprises using an additional pointer operable to identify the first location in the memory where one of the words is stored.* Column 4 lines 39-45 shows that beginning of packet pointer BopPtr 52 points to the beginning of the top packet frame start header 50 as shown in figure 2.

ff. *The location identified by the additional pointer being used as the first pointer when the data packet is flushed.* Column 6 lines 45-48 shows that if a packet is discarded, the write pointer is reset to the value of the beginning of packet pointer for the discarded packet.

18. **Claim 18** is taught by Wang as:

gg. *The method as set forth in Claim 16, further comprising retrieving the data packet from the memory using a second pointer operable to identify a location in the memory where a word is to be retrieved.* Column 4 lines 39-47 shows that read pointer RdPtr 54 points to a location in the buffer for a current read process.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (cited supra).

21. With respect to claim 7, Wang teaches an apparatus as shown supra with respect to claim 1.

22. Wang toes not teach the use of "*a first counter operable to identify a number of data packets stored in the memory*" or "*a second counter operable to identify a number of data packets retrieved from the memory*" as recited in claim 7.

23. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include a first counter operable to identify a number of data packets stored in the memory and a second counter operable to identify a number of data packets retrieved from the memory. The use of counters to track the number of times an event has occurred is well known in the art, consisting of well known circuitry which may be easily implemented by one of ordinary skill.

24. The motivation for doing so would have been to allow the system to track the amount of data packet traffic passing through the system of Wang. This would allow the system or a user of the system to know how much traffic has passed through the network device, which would allow a user to know if the network device is sufficient for the amount of traffic being handled.

25. Therefore, it would have been obvious to include counters for tracking the number of packets received and removed from the FIFO memory of Wang for the benefit of tracking usage of the network device to obtain the invention as recited in claim 7.

26. **Claim 19** is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (cited supra).

27. With respect to claim 19, Wang teaches an apparatus as shown supra with respect to claim 15.

28. Wang toes not teach the steps of "*incrementing a first counter for each data packet stored in the memory*" or "*incrementing a second counter for each data packet retrieved from the memory*" as recited in claim 19.

29. At the time of the invention it would have been obvious to a person of ordinary skill in the art to increment a first counter for each data packet stored in the memory and to increment a second counter for each data packet retrieved from the memory. The use of counters to track the number of times an event has occurred is well known in the art, consisting of well known circuitry which may be easily implemented by one of ordinary skill.

30. The motivation for doing so would have been to allow the system to track the amount of data packet traffic passing through the system of Wang. This would allow the system or a user of the system to know how much traffic has passed through the network device, which would allow a user to know if the network device is sufficient for the amount of traffic being handled.

31. Therefore, it would have been obvious to include counters for tracking the number of packets received and removed from the FIFO memory of Wang for the benefit of tracking usage of the network device to obtain the invention as recited in claim 19.

Allowable Subject Matter

32. **Claims 8, 14, and 20** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

33. **Claims 8 and 14** recite the limitation "*a second comparator operable to compare outputs of the counters and to generate a signal indicating the memory is empty when the outputs are equal*". This limitation, in combination with the other recited limitations of claims 8 and 14, is not taught or suggested by the prior art of record.

34. **Claim 20** recites the limitation "*comparing outputs of the counters and generating a signal indicating the memory is empty when the outputs are equal*". This limitation, in combination with the other recited limitations of claim 20, is not taught or suggested by the prior art of record.

Response to Arguments

35. Applicant's arguments presented at page 12 lines 12-24 of the Appeal Brief filed 9/21/2006 have been carefully and fully considered, and are found persuasive.

36. The additional arguments contained in the Appeal Brief filed 9/21/2006 are considered moot in light of the new grounds of rejection presented supra.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jared I Rutz
Examiner
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DONALD SPARKS
SUPERVISORY PATENT EXAMINER